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| | Filing Date | | 2006-07-19 |
| | First Named Inventor | Dasu, Aravind R. | |
| | Art Unit | 2193 | |
| | Examiner Name | Bullock, Jr., Lewis Alexander Tuan Vu | |
| | Attorney Docket Number | 117316-155055 | |

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| | | | |
|-------|----|---|--------------------------|
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| /VAT/ | 23 | Kuramochi, M., et al. " An Efficient Algorithm for Discovering Frequent Subgraphs" Technical Report 02-026, University of Minnesota, 2002 | <input type="checkbox"/> |
| /VAT/ | 24 | Kwok, Y.K., et al. " Dynamic Critical-Path Scheduling: An Effective Technique for Allocating Task Graphs to Multiprocessors" IEEE Transactions on Parallel and Distributed Systems, Vol. 7, NO 5, May 1996 pp. 506-521 | <input type="checkbox"/> |
| /VAT/ | 25 | Lai, Y.T., et al. "Hierarchical Interconnection Structures for Field Programmable Gate Arrays" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 5. No 2, pp. 186-196, June 1997 | <input type="checkbox"/> |
| /VAT/ | 26 | Lakshminarayana, G., et al. " Wavesched: A Novel Scheduling Technique for Control-Flow Intensive Designs" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No. 5, May, 1999 | <input type="checkbox"/> |
| /VAT/ | 27 | Lee, W. et al. "Space-Time Scheduling of Instruction-Level Parallelism on a Raw Machine", Proc of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), San Jose, CA, October 1998 | <input type="checkbox"/> |
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| /VAT/ | 34 | Mirsky, E. et al. " MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources" IEEE Symposium on FPGAs for Custom Computing Machines, April 17-19, 1996, Napa, CA | <input type="checkbox"/> |
| /VAT/ | 35 | Miyamori, T., et al. " A Quantitative Analysis of Reconfigurable Coprocessors for Multimedia Applications" IEEE Symposium on FPGAs for Custom Computing Machines, 1998 | <input type="checkbox"/> |
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| /VAT/ | 39 | Moreno, J.M. et al. "Approaching Evolvable Hardware to Reality: The Role of Dynamic Reconfiguration and Virtual Meso-structures" Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999 | <input type="checkbox"/> |
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| /VAT/ | 41 | Perchant, A., et al. " A New Definition for Fuzzy Attributed Graph Homomorphism with Application to Structural Shape Recognition in Brain Imaging" hi IMTC'99, 16th IEEE Instrumentation and Measurement Technology Conference, pages 1801-1806 Venice, Italy, May, 1999 | <input type="checkbox"/> |
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| /VAT/ | 48 | Sawitzki, S. et al. "CoMPARE: A Simple Reconfigurable Processor Architecture Exploiting Instruction Level Parallelism" Proc. Of PART, pp.213-224, Springer-Verlag, 1998 | <input type="checkbox"/> |
| /VAT/ | 49 | Schoner, B., et al. " Issues in Wireless Video Coding using Run-Time-reconfigurable FPGAs" Proc of the IEEE Symposium on FPGAs for Custom Computing Machines, Napa CA, April 19-21, 1995 | <input type="checkbox"/> |
| /VAT/ | 50 | Singh, A., et al. " Efficient circuit Clustering for Area and Power Reduction in FPGAs" ACM Transactions on Design Automation of Electronic Systems, Volume 7, Issue 4, October 2002, pp. 643-663 | <input type="checkbox"/> |

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